Translation of

AMENDMENT UNDER ARTICLE 19(35 U.S.C. 371(c)(3))

PCT/JP2004/002714

Amendment of the claims under Article 19(1) (Rule 46)

9. (Additional Claim) A phase comparator circuit for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, said phase comparator circuit characterized in that;

the pulse width of the phase error signal representing the pulse width, as being the phase difference between the transition point of said data signal and the transition point of said clock signal, can be extended by any desired time width.

10. (Additional Claim) A CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filter, operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, and characterized in that;

said phase comparator circuit extends the pulse width of the phase error signal, as being the phase difference between the transition point of said data signal and the transition point of said clock signal, to any desired amount and outputs the phase error signal to said charge pump circuit.

11. (Additional Claim) A phase comparator circuit for operating with a clock signal whose period is equivalent to the unit time width of an inputted data signal multiplied

by any natural number, said phase comparator circuit characterized in that;

the pulse width of the phase error signal representing the pulse width, as being the phase difference between the transition point of said data signal and the transition point of said clock signal, can be extended by any desired time width.

12. (Additional Claim) A CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filer, operating with a clock signal whose period is equivalent to the unit time width of the inputted data signal multiplied by any natural number, and characterized in that;

said phase comparator circuit extends the pulse width of the phase error signal, as being the phase difference between the transition point of said data signal and the transition point of said clock signal, to any desired amount and outputs the phase error signal to said charge pump circuit.